UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/786,049	06/18/2001	Mitsuru Sato	1086.1141	6861

21171 7590 05/13/2004

STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 05/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/786,049	SATO ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. In response to the amendment filed on 02/13/2002:

- the objection to the title has been withdrawn;
- the objections to claims 6 and 11 have been withdrawn;
- the rejection of claims 12 and 16 under the USC 112 2nd paragraph have been withdrawn;
- the rejection of claim 12 under the USC 112 2nd paragraph is maintained and reiterated below for Applicant's convenience;
- the rejection of claims 7-9 and 16 under the USC 112 1st paragraph is maintained and reiterated below for Applicant's convenience.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 4, 7-10 and 15-16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As per claims 4 and 15, both in the specification and claims 4 and 15 of this application, it states that "in the case....the data stored in the cache devices cannot be read without changing its state tag, the data is read without changing the state tag and stored in the cache memory...". It is not understood that if the data stored in the cache devices cannot be read without changing its state tag, then why the data is read without changing the state tag? Claim 10 is also rejected since it is dependent upon indicated rejected claim 4.

As per claims 7 and 16, both in the specification and claims 7 and 16 of this application, it states that "when none of the other cache devices store the corresponding data, the pre-fetch data is invalidated; and when the other cache devices share the corresponding data, the pre-fetch data is stored as it is". It is not understood that if the other cache devices do not contain the data corresponding to the pre-fetch data, then why the pre-fetch data get invalidated?

In the amendment filed on 02/13/2002, the applicant requests to refer to two paragraphs of the specification (i.e. page 8, line 16 – page 9, line 6 and page 39, line 22 – page 40, line 9) for explanation for "invalidating the pre-fetch data when none of the other cache devices store the corresponding data; and storing the pre-fetch data as it is when the other cache devices share the corresponding data". However, the examiner did not find any explanation/description in the cited paragraphs or the remaining specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed

invention. Claims 8 and 9 are also rejected since it is dependent upon indicated rejected claim 7.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claim is generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (USPN: 6,374,330) hereinafter, Arimilli in view of Bourekas et al. (USPN: 6,128,703) hereinafter, Bourekas.

As per claims 1 and 14, Arimilli teaches a cache device set up (28a, 28b in Fig. 1) in each of processors (12a, 12b in Fig. 1) interconnected to other cache devices in other processors and connected to a main memory (16 in Fig. 1), which comprises a

cache memory (28 in Fig. 1) wherein a part of data in the main memory is stored in one or more cache lines and a state tag using to manage data consistency is set up in each of the cache lines and a cache controller (not shown in Fig. 1) for managing transfer of data between the processor and cache memory (e.g. see Col. 1, lines 37-57). However, Arimilli does not teach that the cache controller carries out a weak read operation for causing failure in the pre-fetch request as a fetch protocol. Bourekas, on the other hand, teaches that if the cache line corresponding to the pre-fetch address is in the modified state, then the cache line is invalidated to maintain the cache coherency, i.e. whenever the data/cache line corresponding to the pre-fetch address is in the modified state, that data is most updated data then the data pre-fetched from the main memory. Therefore, the pre-fetched data is invalidated unless the state of the data in the pre-fetch address is changed (e.g. see Col. 10, lines 14-22). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to modify Arimilli's cache device as taught by Bourekas so the cache controller fail the pre-fetch request, in the case of a read request from one of the processors the data stored in the other cache devices cannot be read unless its state tag is changed, to maintain the data consistency. Based on this rationale, claims 1 and 14 are rejected.

As per claim 2, the combination of Arimilli and Bourekas teaches the claimed invention as described above and furthermore, Arimilli teaches that the cache memory distinguishes the stored data by a data-modified state (M), an exclusive state (E), a data-shared state (S) and an invalid state (I), each of which indicates validity of the state

tag (e.g. see Col. 4, lines 14-39). When the data requested by the pre-fetch request is stored in the other cache devices in either the data-modified state (M) or the exclusive state (E), the pre-fetched data is not the most updated data since the data might be changed which is stored in either the data-modified state (M) or the exclusive state (E) in other cache devices. Therefore the pre-fetch request has to fail in order to maintain the data consistency throughout the cache device.

As per claim 3, the combination of Arimilli and Bourekas teaches the claimed invention as described above. In the MESI protocol, which is well known in the art, if the data corresponding to the pre-fetch request is stored in the other cache device in the invalid state, it reads the valid data, which is stored in the main memory and stores it in the exclusive state and if the data corresponding to the pre-fetch request is stored in the other cache device in the shared state, it reads the data from one of those devices since data in those devices is most up-to-date and valid data compare to the main memory data and stores it in the shared state until it modified by that or other cache device to maintain the data consistency. The examiner herein taking Official Notice on this subject matter.

5. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of Bourekas further in view of Prudvi et al. (USPN: 6,378,048), hereinafter, Prudvi.

As per claim 5, the combination of Arimilli and Bourekas teaches the claimed invention as described above and furthermore, Arimilli teaches that the cache memory distinguishes the stored data by a data-modified state (M), an exclusive state (E), a

data-shared state (S) and an invalid state (I), each of which indicates validity of the state tag (e.g. see Col. 4, lines 14-39). However, both Arimilli and Bourekas failed to teach that when the data which corresponds to the pre-fetch request and are stored in the other cache devices is in the data-modified state (M) or the exclusive state (E), the cache controller reads the data without changing the state tag and stores the data in the cache memory with the setup of the weak state (W), and at the time of synchronization operation of the memory consistency the cache controller changes the weak state (W) into the invalid state (I) wholly. Prudvi, on the other hand, teaches that when the data is modified in one of the cache memory, the data is shared without regard to the data's dirty status and data is stored in the cache memory with the setup of the lazy state (L) (similar to the weak (W) state). And at the time of the eviction of that cache memory location, the validity of the data is checked by the dirty bit and invalidated if it is dirty to maintain the cache coherency (e.g. see abstract). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the weak state (W) setup (lazy state (L)) as taught by Prudvi in the cache device taught by Arimilli and Bourekas so the overhead of immediately writing the updated data to the main memory is reduced. Therefore, the performance of the cache device is increased.

As per claim 6, the combination of Arimilli, Bourekas and Prudvi teaches the claimed invention as described above. In the MESI protocol, which is well known in the art, if the data corresponding to the pre-fetch request is stored in the other cache device in the invalid state, it reads the valid data, which is stored in the main memory and

stores it in the exclusive state and if the data corresponding to the pre-fetch request is stored in the other cache device in the shared state, it reads the data from one of those devices since data in those devices is most up-to-date and valid data compare to the main memory data and stores it in the shared state until it modified by that or other cache device to maintain the data consistency. The examiner herein taking Official Notice on this subject matter.

6. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of Bourekas further in view of Gornish et al. (USPN: 5,752,037), hereinafter, Gornish.

As per claim 11, the combination of Arimilli and Bourekas discloses the claimed invention as described above. Arimilli and Bourekas do not teach that when processor sends a read request to the cache controller, the cache controller carries out a pre-fetch request for pre-fetching data in one or more addresses adjacent to a read-requested address after the read request. However, Gornish teaches that when a cache miss occurs, the cache memory device fetches the data requested by the processor from the main memory and at the same time it also pre-fetches the data, i.e. it also fetches the data, which most likely to be called by the processor (i.e. data in one or more addresses adjacent to a read-requested address) in future, and stores this data in the cache (e.g. see Col. 1, lines 25-35 and Col. 2, lines 11-20). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the cache device taught by Arimilli and Bourekas by adding an extra function to the cache controller so it can carry out a pre-fetch request for pre-fetching data in one

or more addresses adjacent to a read-requested address after the read request as taught by Gornish to reduce the number of cache misses because most of the times the next read request sent by the processor is the address adjacent to currently read memory address.

As per claim 12, the examiner interpreted the claim as following: "The cache device according to claim 11, wherein said interconnecting network is a snoop bus". The combination of Arimilli and Bourekas discloses the claimed invention as described above and furthermore Arimilli teaches that the processing units 12a and 12b communicate with each other and the peripheral devices by various means, including a generalized interconnect or bus 20, or direct-memory access channels (e.g. see Col. 1, lines 24-35 and Fig. 1). For example, a snoop bus is used as a system bus 20 for connecting the cache devices 28a and 28b (e.g. see Fig. 1).

7. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of Bourekas further in view of Gornish as applied to claims 11 and 12 above, and further in view of Steely, Jr. et al. (USPN: 5,966,737), hereinafter, Steely.

As per claim 13, although the combination of Arimilli, Bourekas and Gornish discloses the claimed invention as described above, all three Arimilli, Bourekas and Gornish fail to teach that in the case when the simultaneous requests of read and pre-fetch requests arises, the data making the distinguishing bit valid are transmitted. However, Steely discloses that the bit ram is used to provide a bit number of any bit, which differs between the tags at the same location in the different banks (e.g. see abstract). Accordingly, it would have been obvious to one of ordinary skill in the art at

the time of the current invention was made to implement the cache device taught by Arimilli, Bourekas and Gornish by adding the distinguishing bit as taught by Steely to distinguish the data in the case when the simultaneous read and pre-fetch requests occurs and sending the data which makes the distinguishing bit valid. By using the distinguishing bit, sending data requested by the read request to the processor as a response of the pre-fetch request and vice versa can be avoided.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is (703) 305-6219. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HBP
HBP

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 21[illegible]